



**Application Note for  
AnaPico AP3501  
35 GHz High-Speed Sampler  
on Evaluation Board**

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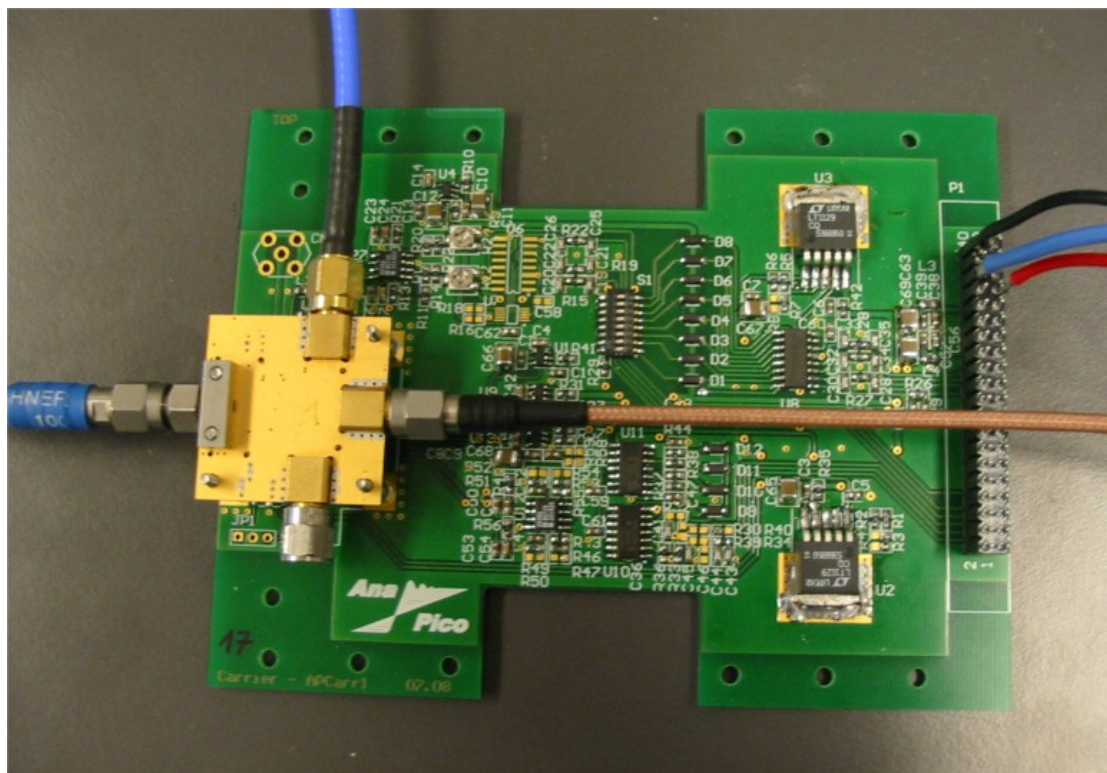
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## 1. Introduction

The AP3501 is delivered in a customized non-hermetic package (approx. size is 30 x 30 x 8 mm) as shown in Fig. 1. The package contains the sampler chip, an IF amplifier, and several decoupling capacitors and resistors. A K-connector is mounted and soldered for the RF input, while SMA connectors serve as LO strobe inputs and IF output. The various bias and supply voltages and the reset signal are applied through contact strips at two sides of the package.

This application note will give an overview how to correctly connect and operate the AP3501 sampler to obtain optimum and reliable performance when used in a customer circuit.

Further information on using the AP3501 sampler mounted on the evaluation board (Fig. 1) is given in section 5.

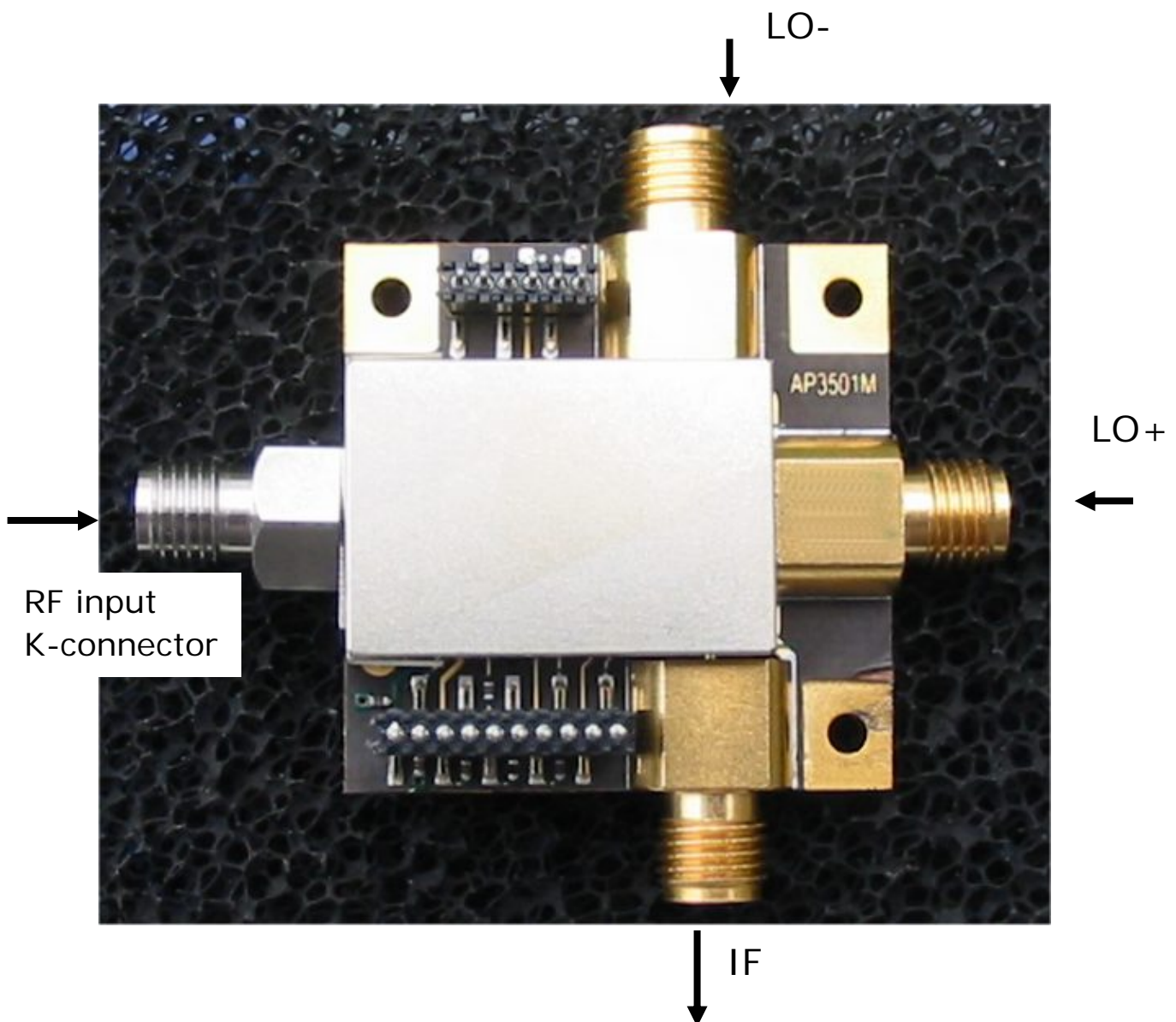


*Figure 1. Evaluation board photo with the AP3501 mounted*

## 2. Electrical Connections to the AP3501

The AP3501 is connected to the measurement setup by several SMA coaxial cables (see Fig. 2) and two contact strips for DC bias voltages.

### SMA/K connectors



*Figure 2. AP3501 module photo showing RF connections*

There are four coaxial connectors attached to the AP3501 as shown in Fig. 2. On the left, a K-connector is used to connect the RF signal. This input is DC-coupled and terminated into 50 Ohms. Two SMA connectors (top and right) connect the differential LO signal. The signals are internally AC-coupled and differentially terminated to 100 Ohms. The third SMA connector (bottom) connects the IF output. It is DC-coupled with an output impedance of 50 Ohms.

### DC bias supply pins

All DC voltages are supplied via two PCB contact strips with a pitch of 1.27 mm (50 mils). Notice to all bias voltages must be applied to guarantee proper operation. In particular, Vcc5 must be supplied to both pin connectors.

There is no special power-up sequence for the voltages except that

**Vcc2 must always be turned on before applying Vcc5 (see also section 4 power up procedure).**

Fig. 3 shows the pin-out of the connectors and Table 1 the nominal bias values, a usable voltage range, and the maximum allowed voltage levels, respectively. Deviation from the nominal bias voltage settings will result in some performance change.

Table 1 Overview of DC supply voltages and signal inputs

Pin name	Nominal operation	Usable range	Damage levels
Vcc5	4.5 V and 160 mA	4.3 to 5.5 V	<b>7 V</b>
Vcc2	6.0 V and 230 mA	5 to 7.5 V	<b>10 V</b>
Vcc3	2.5 V and 7 mA	1 to 3 V	<b>5 V</b>
Vee3	-3.0 V and 10 mA	-4 to -2 V	<b>-6 V</b>
Vee5	-5.0 V	-5.5 to -4.8 V	<b>-7 V</b>
Vbias+	+0.8 V	0 to 2.5 V	<b>-1 or +6 V</b>
Vbias-	-1.4 V	-2.5 to 0 V	<b>-6 or +1V</b>
RF input		-1.5 to +1.5 V	<b>±2Vdc</b>
LON	0.5Vpp	0.25 to 1.5 Vpp	<b>3 Vpp</b>
LOP	0.5Vpp	0.25 to 1.5 Vpp	<b>3 Vpp</b>

Fig. 3 shows the pin assignment for the DC bias voltages.

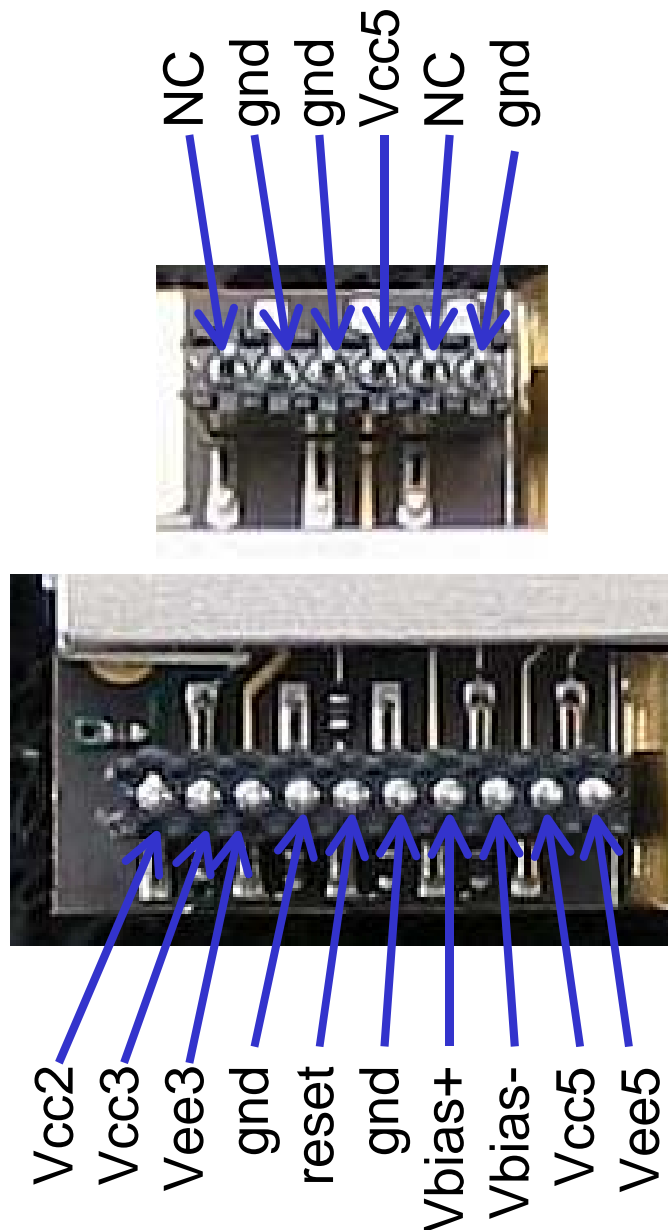


Fig. 3 DC Pin assignment (top view on the sampler module)

The AP3501 generally provides good supply noise rejection with the exception of the sampling diode bias voltages  $V_{bias+}$  and  $V_{bias-}$ . If strong local signals exist within the IF bandwidth of the sampler (e.g. broadcast transmitters), extra external filtering in the  $V_{bias+}$  and  $V_{bias-}$  lines may be required.



The AP3501 contains bias decoupling capacitors to GND on all bias lines.

## RF, LO and IF signals

**LO signal:** The preferred mode of operation is using differential LO signals. A 0.25 to 1.5 V peak-peak signal per branch should be applied to guarantee optimum performance. Skew between positive and negative signal branches should be as low as possible ( $\ll 100$  ps). Due to the internal AC-coupling of the LO inputs it is recommended to operate the LO not lower than 100 kS/s. The upper limit for the sampling rate is above 600 MS/s. Sampling rates below 100 kS/s are only possible by removing the internal AC coupling at the LO input ports.

Single-end operation is also possible. When using a single-ended LO, the other LO input should be terminated to  $50 \Omega$  or GND. For single-ended operation, the LO amplitude should be  $< 1$  V<sub>pp</sub>.

**IF output:** The IF output is DC-coupled and the output impedance is  $50 \Omega$ . The IF output is not sensitive to short-circuits.

## 3. Sample-Hold and Sample-Hold-Reset Operation

The AP3501 has two operating modes, the sample-and-hold and the sample-hold-reset mode, respectively.

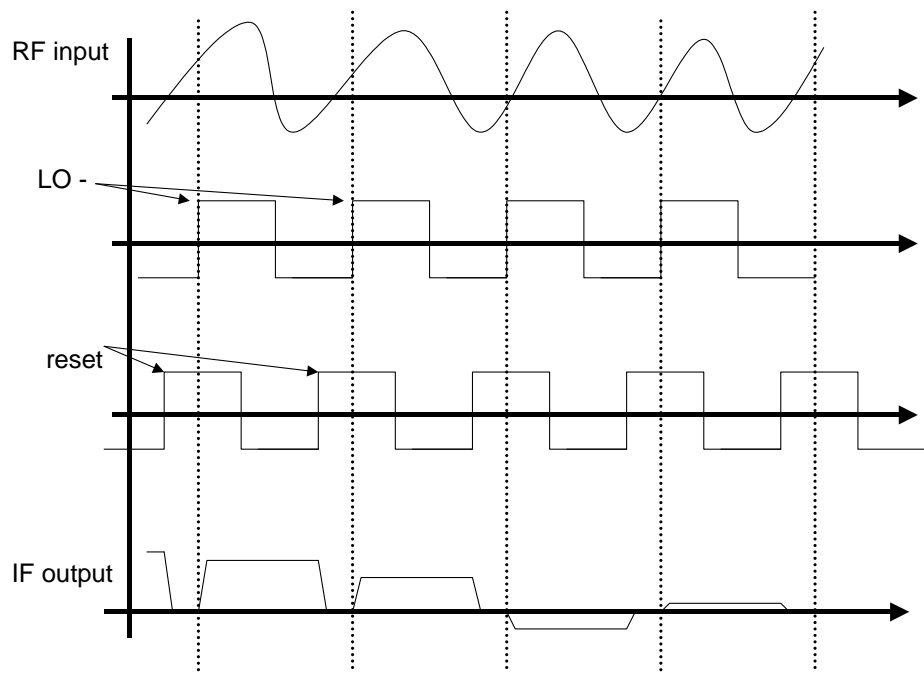
If the "reset" pin is left unconnected (or connected without applying an AC reset signal), then the **sample-and-hold** mode is active. The sampler holds the sampled voltage at the IF output until the next sampling strobe occurs. Parasitic discharge time constant is much higher than one over the lowest recommended sampling rate. After another sampling strobe, the IF output changes. Since the conversion efficiency of the intrinsic sampler is not 100%, any sample presented at the IF output is a function of the previous sample and the RF voltage during the sampling aperture. Thus the sampler is said to have a memory, which in some applications is not desired.

Then instead the **sample-hold-reset** mode can be used. To use this mode, a reset signal must be applied at the reset pin. Fig. 4 shows schematically the timing sequence. On the rising edge of the LO- (negative branch) a instantaneous sample of the RF waveform is captured and displayed at the IF output. The IF output is hold until a positive edge of the reset signal occurs. The IF output is reset to a constant voltage and remains there until, with the next rising edge of the LO- occurs. A “memory-free” operation is enabled.

The delay between the pos. edge of the LO- and the reset signal determines the duty cycle of the IF output.

Now there are some timing restrictions that apply, particularly if operated at high sampling rates (e.g. 50 MHz). The delay must be selected such, that the IF output has sufficient time to settle to the new sampled voltage and can be read by the following signal processing stages. On the other side, if the delay is too large, then the reset operation is not completed before the next sample is sampled. This leads to a unpredictable operation.

The duration of the reset operation is affected by the reset signal amplitude. For fast resets, an amplitude of 0.2 to 0.4 V and a fast rise time (< 0.5 ns) are recommended.



*Fig. 4 Timing diagram for the sample-hold-reset operation*



## 4. Power Up Procedure

Before powering up the AP3501 evaluation board, **please read and follow these general recommendations:**

- *Place the AP3501 such that a good thermal dissipation is guaranteed. The AP3501 does not require any dedicated heat sink.*
- *Before applying any RF and DC signals, make sure that all DC and SMA cables are in place.*
- *Avoid unnecessary mechanical stress especially at the DC bias connectors. De-lamination of the contacts may result from excessive stress.*
- *The AP3501 is a high-speed device with limited ESD protection. Especially the RF and LO inputs are susceptible to ESD damage.*

Please use the following power-up sequence to guarantee save and reliable operation of the AP3501:

- Attach the DC and the appropriate RF connectors
- Turn on supply Vcc3 and Vee3
- Turn on supply Vbias+ and Vbias-
- Turn on supply Vcc2
- Turn on supply Vcc5 and Vee5
- Apply LO and RF signals

The AP3501 is not sensitive to the exact order of the supplied DC and AC signals. But there is one exception:

**ALWAYS TURN ON Vcc2 BEFORE Vcc5 AND TURN OFF Vcc5 BEFORE Vcc2!**

There may be reliability issue if Vcc5 is turned on before Vcc2.

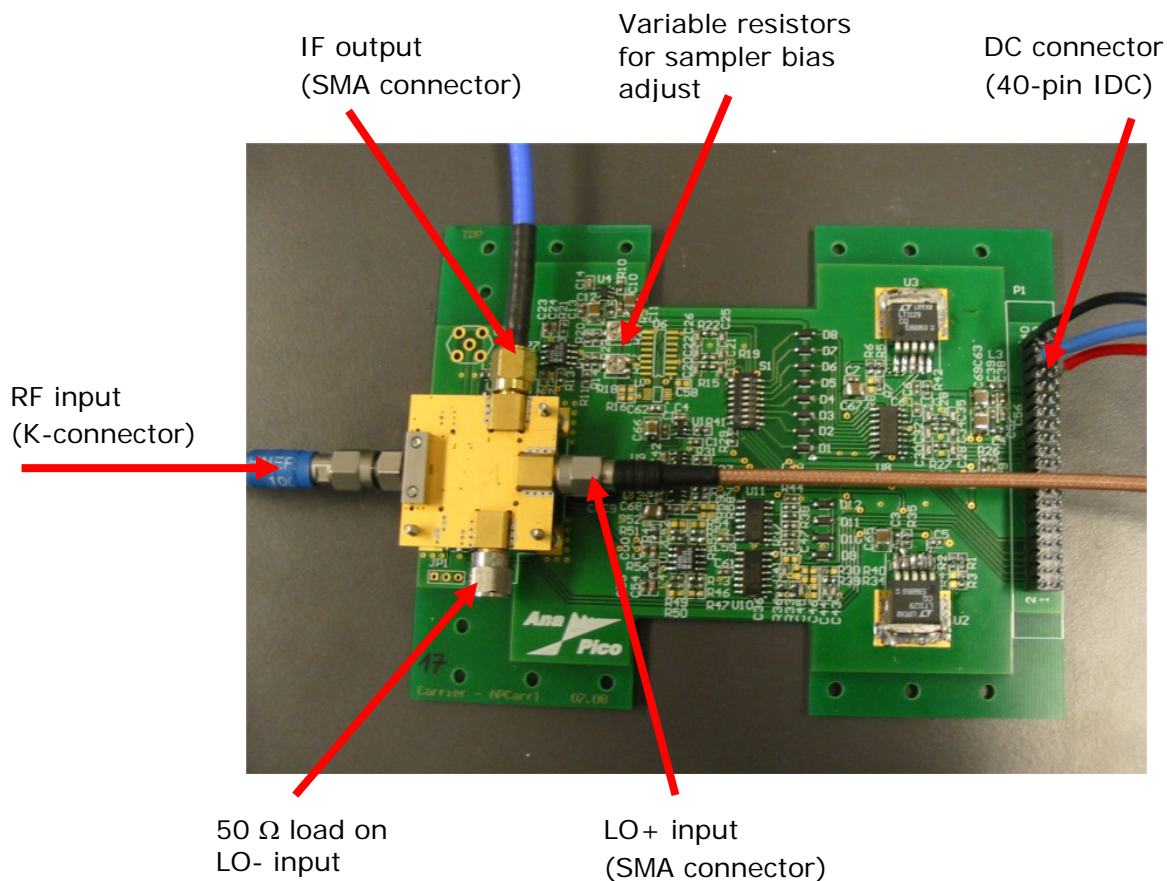
## 5. Using the Manual Sampler Evaluation Board

The AP 3501 sampler module is mounted upside down on the evaluation board and held in its position by three M2-screws.

The RF connections are all made by coaxial cable and labeled in Fig. 5. This figure shows the sampler driven with a single-ended LO-drive, with the second LO-drive input terminated by a  $50\ \Omega$  load.

The evaluation board is fitted with two variable resistors that control the bias voltages  $V_{bias+}$  and  $V_{bias-}$  applied to the sampler.

The pinout of the 40-pin IDC connector is shown in Fig. 6.



*Fig. 5: Sampler evaluation board showing RF and DC connections and the variable resistors for setting the sampler bias voltages*



Inductors L1 and L2

sampler bias adjust trimpot (not populated on photo)

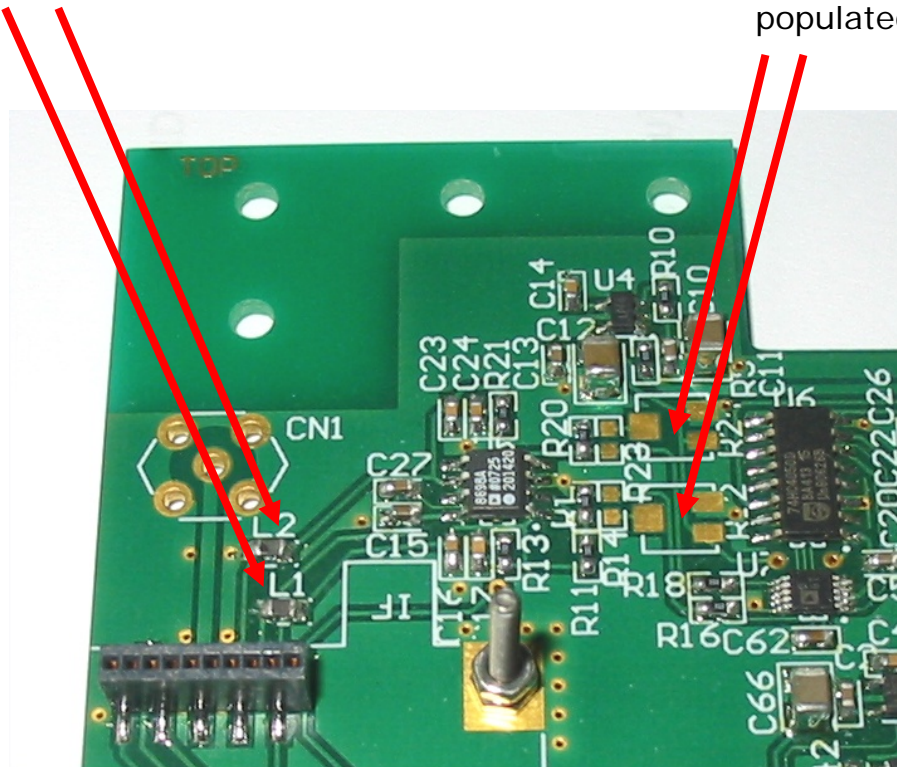


Figure 7: Location of variable resistors for manual sampler bias adjust, and location of L1 and L2 where the sampler bias voltages can be checked.

## 7. Document History

Version/Status	Date	Author		Notes
V10	2006-9-9	jk		first draft
V11	2007-04-16	ul		editorial update
V12	2007-12-13	ul		evaluation board section added
V13	2008-06-25	ul		manual bias adjust added