Application Note AN6002

APVSG Fast Control Port

Purpose

For fast, time critical settings and data streaming the APVSG can be controlled over an additional port. This application note explains the configuration and usage of the Fast Control Port.

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Introduction

The fast control port is a parallel port with the possibility for the user to control specific aspects of the IQ modulation of the APVSG. When activated, the FCP can be configured to operate in one of two main modes. The interface is set to stream either IQ data or memory segment addresses.

Setting the FCP in the former mode allows the user to stream IQ data to the APVSG directly and thus modulate the carrier frequency, as depicted in Figure 1. The FCP operates source synchronously and expects to receive IQ data in single data rate (SDR) along with a 250MHz clock.

Instead of streaming the IQ modulation data directly through the FCP, the modulation data can also be replayed from the local APVSG IQ memory. When the FCP is configured in segment mode, it provides the option to choose the replayed IQ data. By streaming the address of the memory segments of the desired IQ data, the user is thus able to directly switch between different stored IQ data.

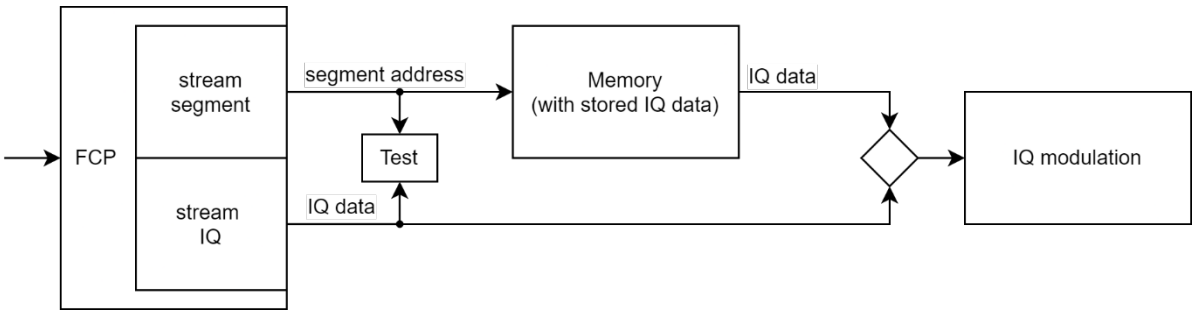

Figure 1: Functional diagram of FCP in APVSG with non-FCP parts omitted.

FCP operation modes

The fast control port (FCP) supports two main use-cases:

- Data streaming to the device for IQ modulation
- Selecting memory segments of the internal RAM

To select the operating direction of the Fast Control Port, the FCP must be configured with the following SCPI commands:

[:SOURce]:FCPort:STReam:SEGment OFF|ON|0|1

Sets the FCP to stream address segments.
*RST value: OFF

[:SOURce]:FCPort:STReam:IQ OFF|ON|0|1

Sets the FCP to stream IQ data.
*RST value: OFF

[:SOURce]:BB:ARBitrary:FCP[:STATe] OFF|ON|0|1

Sets the FCP as source for IQ.
*RST value: OFF

Further related commands are documented in the Programmer's Manual[1] and application examples can be found on the following pages of this application note.

IQ data streaming with FCP

The FCP can be set as an input for IQ modulation data which is then directly applied to modulate the carrier frequency. To configure the device to receive IQ data on the FCP, the FCP must be set into IQ streaming mode and the FCP must be set as the source of the IQ modulation data.

The FCP for the source-synchronously clocked IQ streaming consists of 16 IQ-data bits, a valid bit, and a clock. The clock is a continuous 250 MHz signal with the valid bit and IQ data transmitted in single data rate (SDR) which results in 125 Mega samples per second of IQ data.

Limitations and requirements:

- A stable frequency of fixed 250MHz is required on the clock pin of the FCP.
- Data at the FCP input must be streamed at 125Msps SDR.
- It is recommended to operate the sender (that clocks the 250MHz clock and the IQ data) and the APVSG at the same reference clock to avoid undesired frequency offset effects.

Setup FCP for IQ data streaming

Configuration steps prior to transmission

1. Connect an external reference clock (recommended).
2. Connect the FCP input on the device.
3. Send stable 250MHz clock signal on the FCP connector clock pins (see electrical specification for details on pin placement)

Complete SCPI command sequence for IQ stream input on FCP:

ROSC:EXT:FREQ<x>	Sets the reference frequency (recommended)
ROSC:SOUR EXT	Sets the reference to external (recommended)
FREQ <x>	Sets initial RF output frequency
OUTP:STAT <x>	Sets RF output
FCP:STR:IQ ON	Sets FCP to IQ stream mode
BB:ARB:FCP ON	Sets FCP as source of the IQ modulation data

Related SCPI Commands

[:SOURce]:FCPort:STReam:IQ OFF|ON|0|1

Sets the FCP to stream IQ data.
*RST value: OFF

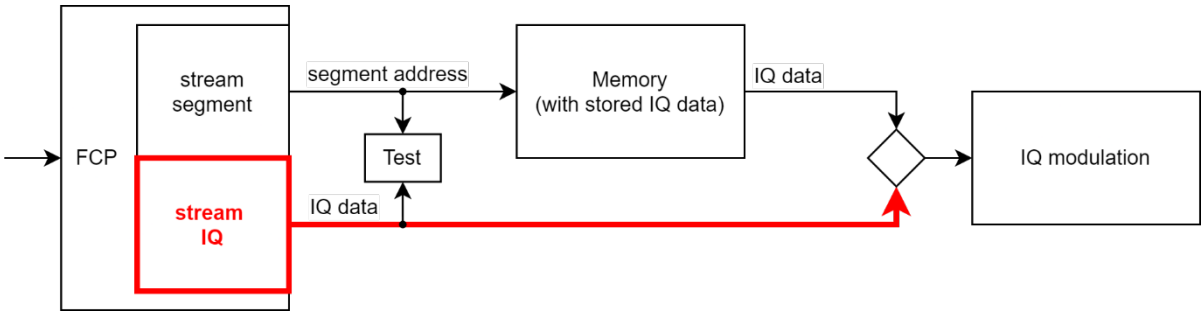

Figure 2: The FCP:STR:IQ SCPI command determines if the FCP is in IQ streaming mode. The received data is then forwarded to potentially modulate the carrier frequency. Note that this mode can only be enabled if no other FCP mode is enabled simultaneously.

[:SOURce]:BB:ARBitrary:FCP[:STATe] OFF|ON|0|1

Sets the FCP as source for IQ.

*RST value: OFF

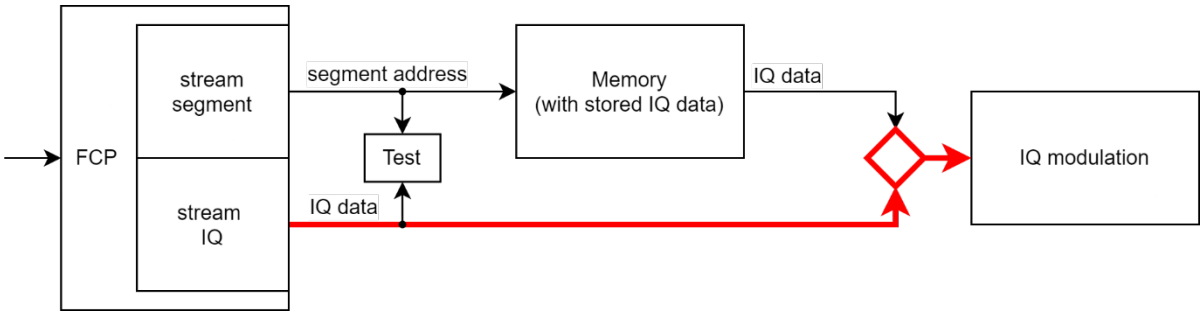

Figure 3: The BB:ARB:FCP[:STAT] command decides if the FCP IQ data is forwarded for IQ modulation. This command only takes hold if the BB:ARB:WAV:STAT command is not enabled simultaneously.

IQ Stream Timing

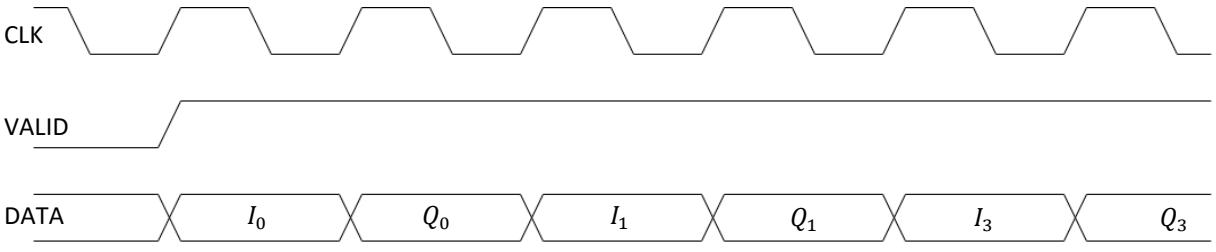

Figure 4: IQ stream input timing for the fast control port (FCP)

The FCP receives a valid signal that is synchronized with the first valid I-data sample, followed by the first Q-data sample. The valid signal should be driven low during the setup of the device to ensure proper sampling of I and Q data samples.

The phase relationship of input signals to the FCP are depicted in Figure 4. See the electrical specifications for details on pin assignment at the MDR 36-pin connector.

Clock and data edges are transferred at the same time. The FCP reads the data upon each rising edge of the clock. The input delay between data and clock inside the APVSG can be adjusted slightly in order to optimize and relax the sampling of the IQ data.

SCPI & FCP Example

This is a SCPI example to set the FCP. Make sure to follow the steps prior to transmission as described in section *Setup FCP for IQ data streaming*.

ROSC:EXT:FREQ 10e6	Sets the reference frequency to 10 MHz
ROSC:SOUR EXT	Sets the reference to external
FREQ 50e6	Sets initial RF output frequency 50 MHz
OUTP:STAT ON	Enables RF output
FCP:STR:IQ ON	Sets FCP to IQ stream mode
BB:ARB:FCP ON	Sets FCP as source of the IQ modulation data

After successfully configuring the device, the IQ modulation data (e.g. a 1-tone) can be sent to the FCP - make sure the valid signal is synchronized to the first 16-bit I-data sample. A valid input IQ stream results in a modulated carrier frequency at the RF output. You can now

- Set some frequency with FREQ <x>.
- Send another IQ modulation e.g. 2-tone to input of FCP.
- Watch the output being modulated.

If you have trouble setting up the FCP to correctly receive your IQ data, have a look at section *FCP Test mode*. The FCP IQ streaming comes with an integrated testing mode that can help detect the most common issues in your setup.

Selecting memory segments

The fast control port (FCP) can be configured to receive memory segment IDs to select desired memory segments for playback. When the FCP is configured in segment selection mode, the FCP cannot be configured to run in any other mode simultaneously.

The FCP expects a 16-bit wide memory segment ID, as well as a valid signal that indicates when a new ID is valid at the FCP.

Setup for Selecting Memory Segments

The configuration steps for segment streaming to FCP are straight forward.

1. Connect the FCP input at the connector on the APVSG.
   See the electrical specifications section for pin mapping on the connector.
2. Set the FCP to IQ stream mode with the SCPI command
   FCP:STR:SEG ON

FCP Segment SCPI Commands

[:SOURce]:FCPort:STReam:SEGment OFF|ON|0|1

Sets the FCP to stream segments IDs.

*RST value: OFF

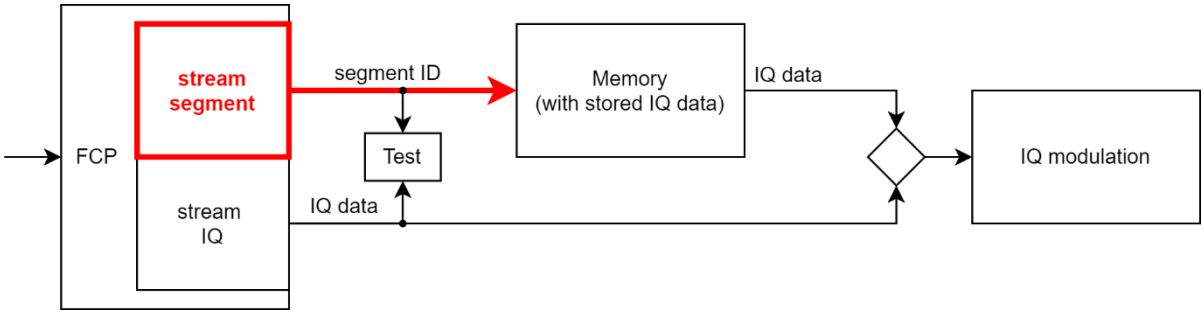

Figure 5: The FCPort:STReam:SEGment command determines whether the FCP is streaming memory segment IDs. Note that this mode can only be enabled if all other FCP modes (e.g. stream IQ) are turned off.

Segment Stream Timing

The FCP receives a valid signal that is synchronized with the data. Each new segment ID is to be accompanied by a rising edge of the valid signal. The valid signal should be driven low during the setup of the APVSG.

The temporal relationship of the input signals to the FCP are depicted in Figure 4. See the electrical specifications for details on pin assignment at the connector, where Addr is an alias for segment ID.

Segment IDs and valid bit edges are transferred at the same time. The FCP reads the input with a sampling rate of 250 Mbits per second for each signal which naturally limits the switching of the valid signal to every 4ns the earliest.

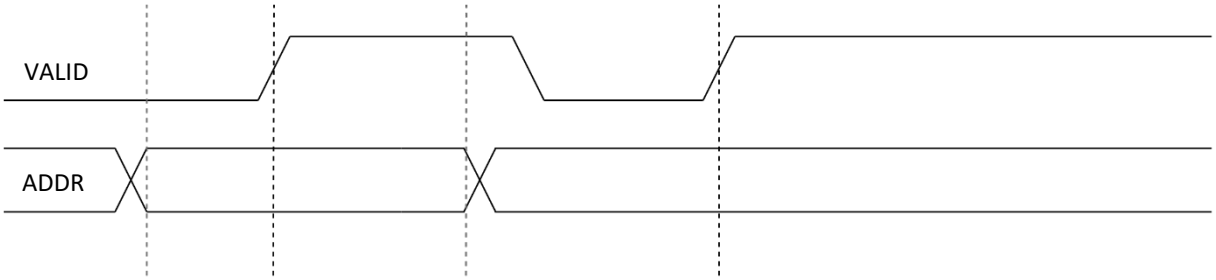

Figure 6: Timing diagram for memory segment inputs (not to scale)

SCPI & FCP Example

1. Write some IQ data to the internal memory of the APVSG, e.g. a 1-tone modulation. This can be done by e.g. uploading the data of a QI file with the APVSG GUI.
2. You can use either the GUI or the following SCPI commands to further setup the APVSG.

FREQ 50e6	Sets initial RF output frequency 50 MHz
OUTP:STAT ON	Enables RF output
FCP:STR:SEG ON	Sets FCP to segment stream mode
BB:ARB:WAV:STAT ON	Sets RAM as source of the IQ modulation data

After successfully configuring the device, the segment ID can be sent to the FCP - make sure the positive edge of your valid signal is sent along with the 16-bit segment ID signal. You can now

- Set some frequency with FREQ <x>.
- Send a different segment ID with a new positive edge on the valid signal to switch the IQ modulation data replayed from the RAM.
- Watch the output being modulated accordingly.

FCP Test mode

The following sections describe the behaviour of the FCP in test mode. For each streaming mode of the FCP the functionality of the test varies to account for the type of transmission employed in the specific streaming mode.

There are two SCPI commands for FCP testing. One command to enable or disable the test mode for FCP and a second command to print the related information on the active FCP streaming mode and the testing of this mode.

Related SCPI Commands

[:SOURce]:FCPort:TEST OFF|ON|0|1

Sets the FCP to test mode.

*RST value: OFF

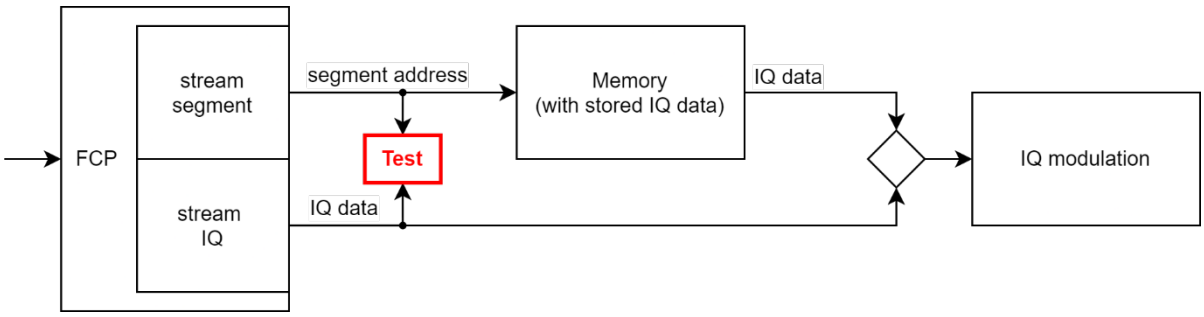

Figure 7: The FCP:TEST command dictates if the FCP is being run in test mode. Please note that the behavior of the FCP test depends on the applied streaming mode at any given time.

[:SOURce]:FCPort:DIAGnostic

Prints diagnostic information regarding the FCP.

The displayed information varies according to streaming mode. When the FCP test mode is activated, the test information and results are show along with the diagnostic information on the current FCP state.

FCP IQ Stream in Test Mode

The diagnostic information for the FCP relays the state of the received clock on FCP. For the FCP to be able to sample the IQ data correctly in IQ streaming mode, the respective clock pin must be driven with a stable 250 MHz signal with 50% duty cycle. The FCP will only be able to lock onto the clock signal if it is stable. Consult the FCP:DIAG SCPI command to check if your applied clock signal meets these requirements. Please note, that it is recommended to drive this clock signal and the reference clock for the APVSG with the same source clock.

Once a sufficient clock signal is applied, the IQ data can be tested for correct transmission. The FCP IQ stream mode contains a built-in test that makes use of a linear feedback shift register (LFSR) to generate a pseudo-random test pattern for the I-data and the Q-data separately. Thus, all combinations of the 16-bit IQ data are tested except for the 0x0000 combination. In the following, the iterations to generate the test pattern are described in pseudo code.

```
// initialize I and Q
i_0 = 0x306C;
q_0 = 0xFFFF;
do { // for each iteration.
    i = i XOR (i << 7);
    i = i XOR (i >> 9);
    i = i XOR (i << 8);
    q = q XOR (q << 7);
    q = q XOR (q >> 9);
    q = q XOR (q << 8);
}
```

Which will result in:

$$\mathrm{I}_0 = 0\mathrm{x}306\mathrm{C}, \mathrm{Q}_0 = 0\mathrm{xFFFF}, \mathrm{I}_1 = 0\mathrm{x}696\mathrm{F}, \mathrm{Q}_1 = 0\mathrm{x}7\mathrm{F}7\mathrm{F}, \mathrm{I}_2 = 0\mathrm{x}5\mathrm{E}80, \mathrm{Q}_2 = 0\mathrm{x}5\mathrm{F}9\mathrm{F}, \ldots$$

The built-in comparator will wait for the initial pattern of I_0 and Q_0 to start comparing the received data. Make sure the valid bit you send to the FCP is high during the transmission of the test patterns or the FCP will not recognize the data as valid input. Also take care to send the rising edge of the valid bit simultaneously with an I-data as described in section *IQ Stream Timing.*

The comparator will then compare the data on the FCP input as long as it is valid and count the numbers of errors detected for each bit. The pattern comparison will stop if the valid bit is low and resume when it is high again. The diagnostic information of the FCP that can be accessed with the FCP:DIAG command gives information on the state of the valid signal, the test comparison and the amounted errors. The displayed number of errors per bit are limited to 2^{21} and will overflow if excessed. Furthermore, the presented values do not necessarily represent an exact point in time since the error counts for the separate bits are gathered consecutively and not simultaneously.

Example of a possible FCP:DIAG response:

```
******* FCP diagnostic:
        FCP State : IQ Stream (Slave)
        FCP clock : locked and frequency OK
        FCP Data  : valid

        FCP Test  : enabled
        Test State: comparing patterns
        Current error count of each bit:
        D15:    D14:    D13:    D12:    D11:    D10:    D09:    D08:
              0       0       0       0       0       0       0       0
        ------------------------------------------------------------
```

```
D07:    D06:    D05:    D04:    D03:    D02:    D01:    D00:
      0       0       0       0       0       0       0       0
```

FCP Segment Stream in Test Mode

The test mode for memory segment address stream is a lot simpler than for the IQ streaming mode. Since the transmission is not source synchronous but the data is sampled at the FCP input, there is only diagnostic information about the valid bit and the received address.

In test mode, the address input is directly forwarded to the diagnostic information along with the state of the valid bit.

Example of a possible FCP:DIAG command response:

```
******* FCP diagnostic:
        FCP State : Segment Stream (Slave)
        FCP ready : 1

        FCP Test  : enabled
        FCP Data  : valid
        FCP Input : 0xA1C4;
```

Cable Assembly

The specifications for the connecting cable on the FCP port vary depending on the deployed use-case of the FCP. For recommendations on parts for a custom cable for either IQ streaming or segment address streaming, please contact your AnaPico representative directly.

Further Documentation

[1] AnaPico Programmer's Manual for Signal Generators
https://www.anapico.com/downloads/manuals/